

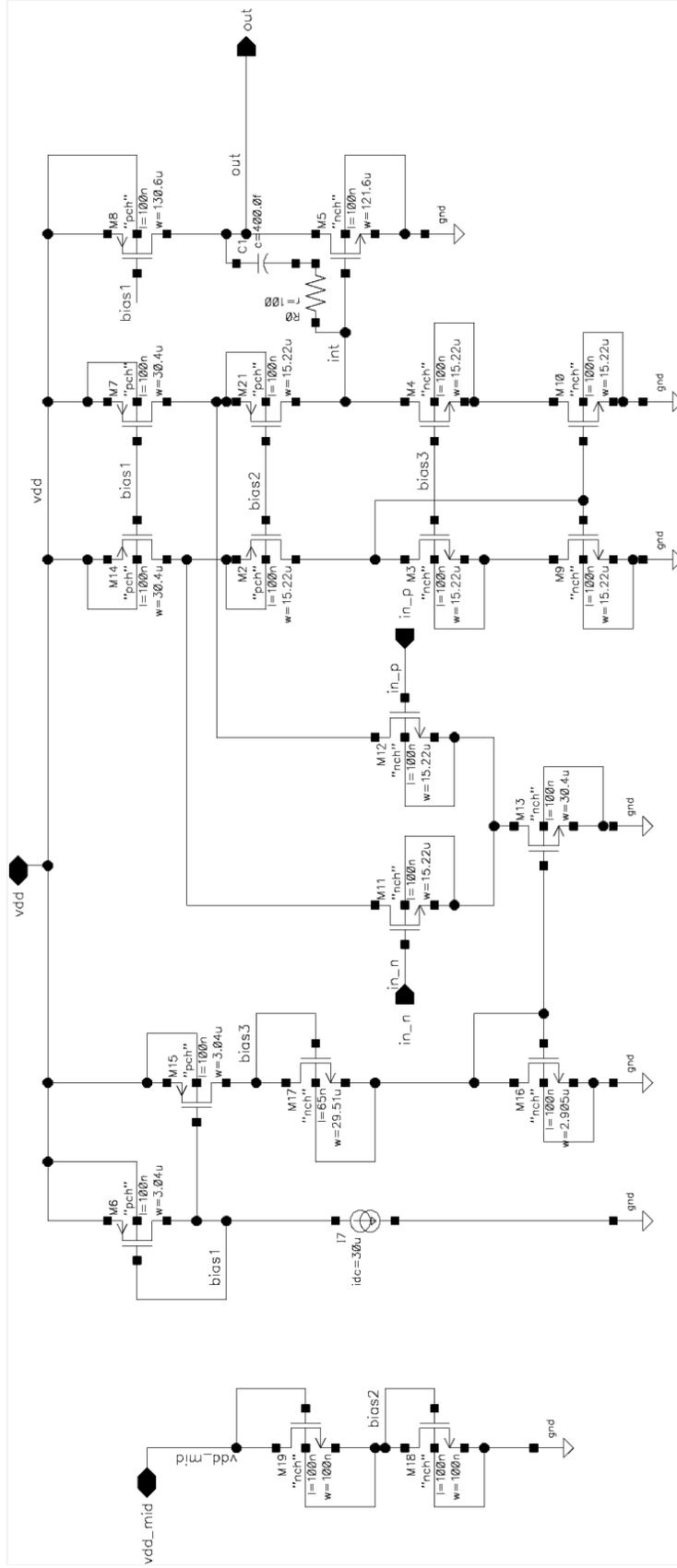
6.775 Midterm Project
65nm CMOS op amp design

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Folded Cascode – Common Source Amplifier



2 Specifications

Specification	Requirement	This design	Notes
1. Settling Time (0.1%)	8ns max up/down	5.3ns (up)	4.8ns down
2. Power Consumption	3mW	2.42mW	
3. Output resistance	1Ω	0.28 Ω	Closed loop, small sig
4. Thermal Noise	400uV RMS	308uV RMS	Output referenced, 10kHz-500MHz
5. Small signal gain	5,000	6,168	No load, DC
6. Output Swing	0.2V – 1.0V	0.068V-1.09V	No-load
7. Phase Margin	60°	73.8°	1pF load, gain of 2
8. PSRR+ (vdd)	60dB at DC 40dB at 50KHz	100.1dB at DC 100.0dB at 50KHz	
9. CMRR	60dB	80.3dB	At Vcm = 0.6V

Component Details (left to right on schematic)

All transistors have L=100nm except M17, which has L=65nm.

RefDes	Type	Size	Notes	RefDes	Type	Size	Notes
M19	Nch	W=100nm	Bias2 gen	M14	Pch	W=30.4um	I source
M18	Nch	W=100nm	Bias2 gen	M7	Pch	W=30.4um	I source
M6	Pch	W=3.04um	Bias1 gen	M2	Pch	W=15.22um	Cascode
I7	I source	30uA	Reference current	M21	Pch	W=15.22um	Cascode
M15	Pch	W=3.04um	I mirror	M3	Nch	W=15.22um	Cascode I source
M17	Nch	W=29.51um	Bias3 gen	M4	Nch	W=15.22um	Cascode I source
M16	Nch	W=2.9um	Bias	M9	Nch	W=15.22um	Cascode I source
M11	Nch	W=15.22um	Diff Pair	M10	Nch	W=15.22um	Cascode I source
M12	Nch	W=15.22um	Diff Pair	R0	Resistor	R=100 ohm	Comp
M13	Nch	W=30.4um	I source	C1	Capacitor	C=400fF	Comp
				M8	Pch	W=130.6um	I source
				M5	Nch	W=121.6um	Gain

Hand Design

The initial design topology was performed based on consideration of gain, settling time, and phase margin specifications, and power supply voltage and current constraints. A folded cascode topology was chosen based on high gain with reasonable device sizes, allowing for high bandwidth.

Gain

The first stage of this amplifier (folded cascode) provides a gain equal to $\frac{(g_m r_o)^2}{4}$ due to the current gain of the differential pair and output resistance of cascode stages and active load. The second stage provides $\frac{g_m r_o}{2}$ due to the current gain of the nmos and the parallel output resistance of the gain transistor and the active load current source. Therefore the total gain of the amplifier is $\frac{(g_m r_o)^3}{8}$. The gain target is 5000, I will choose conservatively 6000 for engineering margin. This requires transistors with a gain of $\sqrt[3]{6000 * 8} = 36.3$.

Settling Time

Settling time from a step input is based on Gain-bandwidth of the amplifier. Required GBW is determined by $k = e^{\frac{-T_s}{\tau}}$. This gives a GBW = $-\ln(0.001)/(8ns) = 875\text{MHz}$. For adequate phase margin, Ft of the transistors is desired to be 10X the unity gain bandwidth, so this is set at $\sim 8.7\text{GHz}$.

Gm requirements

The compensation capacitor is conservatively set to be equal to one half the load capacitance, or 0.5pF. Gm of the first stage is determined by the corresponding pole, and is equal to

$$Gm_1 = (875\text{MHz}) * (2\pi \text{ rad/Hz}) * (0.5\text{pF}) = 2.74\text{mS}.$$

Gm of the second stage is determined by the corresponding pole, and is equal to

$$Gm_2 = 4 * \frac{C_l}{C_c} * Gm_1 = 21.9\text{mS}.$$

Based on requirements for Gm (2.74mS and 21.9mS), Ft (8.7GHz) and gain (36.3), the transistors were chosen to have a length of 100nm and current density of 10uA/um for both PMOS and NMOS. This was chosen graphically based on small signal parameters derived by OCEAN script, parameters given below. Vdsat was also taken into consideration to allow for reasonable device headroom within power supply voltage, in order to meet output swing specification.

Device	Gm/um	Ft	Gain	Vgs-Vt for desired current density	Vdsat
NMOS	0.18 mS/um	28GHz	41	382mV	62mV
PMOS	0.12 mS/um	11GHz	31	470mV	150mV

Input stage gain transistor sizing

The width of the input stage M11 and M12 was chosen based on the above gm/um and required Gm. This results in

$$W = \frac{2.74mS}{0.18 mS/um} = 15.22um$$

The wide input transistors also provide for low noise, with noise from the input transistors dominating overall noise. This is important because noise from the first stage is amplified and directly reflected in input-referred noise. This will be discussed in more detail later. Based on this width and the chosen current density, the current in each transistor M11 and M12 is

$$15.22um * \frac{10uA}{um} = 152.2uA$$

First stage Differential Pair tail current source sizing

The current through the tail current source M13 is equal to double the current through each transistor M11 and M12, or 2*152.2uA = 304.4uA. Based on the chosen current density, this gives the width of M13 as

$$W = \frac{304.4uA}{10 uA/um} = 30.4um$$

First stage cascode / current source transistors sizing

The current through the folded cascode leg of the first stage (M2, M21, M3, M4, M9, M10) is chosen to be equal to the current in each differential pair transistor, or 152.2uA per leg. This results in a width for these transistors which is equal to the differential pair transistors, or 15.22um.

First stage PMOS current source transistors sizing

The PMOS current source transistors M14 and M7 supply current which is shared between the differential pair leg and the cascode leg. Because these legs are equal in current at 152.2uA, the current supplied by these PMOS transistors is double this current, or 304.4uA. Based on the chosen current density, this gives the width for M14 and M7 as

$$W = \frac{304.4uA}{10 uA/um} = 30.4um$$

Second stage gain transistor sizing

The width of the second stage gain transistor M5 was chosen based on the above gm/um and required Gm. This results in

$$W = \frac{21.9mS}{0.18 mS/um} = 121.6um$$

Based on this width and the chosen current density, the current in the second leg is

$$121.6um * \frac{10uA}{um} = 1216uA$$

Second stage current source transistor sizing

The PMOS current source M8 must supply the second stage with 1216uA (calculated above). Based on the chosen current density, this gives a width equal to

$$W = \frac{1216\mu A}{10 \mu A/\mu m} = 121.6\mu m$$

This value was adjusted after simulation to minimize systematic offset.

Current reference and transistor sizing

The current source I7 value was chosen as 30uA for minimal power overhead. The reference transistor M6 sizing is given by the relative currents and width ratios:

$$\frac{I_{ref}}{I_{desired}} = \frac{30\mu A}{304\mu A} = \frac{\frac{W}{L}_{ref}}{\frac{W}{L}_{desired}} = \frac{\frac{W}{L}_{ref}}{304}$$

Therefore, with L=100nm the width of M6 is equal to 3.04um. The node bias1 supplies the bias to the PMOS current sources.

Current mirror and input pair current source bias transistor sizing

As described before, current is sunk from the input differential pair by an NMOS transistor M13. M13 is biased by a current mirror comprising of M15 (PMOS) and M16 (PMOS). These transistors are sized such that the current through this leg is 30uA for minimal power overhead. This also provides the bias voltage to M13 based on the W/L ratios as before, at 300uA. Therefore, M15 and M16 are sized to be equal to M6 at W=3.04um. The width of M16 is adjusted in the real design, see below. The bias voltage is approximately 382mV as determined above.

Cascode transistor biasing

Based on the above choice of current density, the desired DC operating point of the first stage output is 382mV. The cascode transistors M3/M4 in the NMOS current sink can be thought of in terms of bias as source follower transistors. Their bias voltage (bias3) is equal to Vds of the lower transistors M9/M10 plus Vgs required for desired current density. To keep M9/M10 in saturation Vds > 62mV. Therefore, bias3 > Vds,sat + Vgs = 62mV + 382mV = 444mV. This is the lower bound for bias3. It's known that the DC output of the first stage must be equal to 382mV to properly bias the second stage. Because transistors M3/M4/M9/M10 are carrying equal current densities, and Vd(M4)=382mV, Vd(M9/M10) is approximately half of this, or 191mV. Therefore, bias3 is approximated to be 382+191 =573mV. The real value was determined by simulation in order to set the desired operating point of the first stage output, and was found to be bias3=620mV. Bias3 is generated by a diode-connected transistor M17 inserted into the current mirror. With the source voltage of M17 equal to 382mV (see above), for M17 Vds=Vgs=620mV-382mV=238mV. As determined by a Vgs versus drain current density from OCEAN plot, an appropriate choice of size for M17 is L=65nm, W=29.51um. This was also adjusted in simulation. M16 was also adjusted in size based on simulation, due to the addition of M17.

The PMOS cascode transistors M2 and M21 are also biased for the desired current density, with $V_{gs} = 470\text{mV}$. They also act as source followers, and the bias point is constrained to keep PMOS current source transistors M14 and M7 in saturation ($V_{dsat} = 150\text{mV}$). Therefore, the upper bound of the bias point bias2 is $1200\text{mV} - 150\text{mV} - 470\text{mV} = 580\text{mV}$. It is known that the drain voltage of M21=382mV for proper biasing of the second stage. Because PMOS transistors M14/M7/M2/M21 are carrying equal current densities, it is approximated that their V_{ds} 's are equal. Therefore, the voltage of the internal node between M7/M21 or M14/M2 is approximately $1200 - (1200 - 382)/2 = 795\text{mV}$. Therefore, by subtracting V_{gs} for the PMOS transistors, the appropriate bias point for transistors M2/M21 is $795 - 470\text{mV} = 325\text{mV}$. The final value was determined by simulation to be 300mV. 300mV for bias2 was generated by a transistor voltage divider from the mid-rail reference of 600mV. Small transistors M18, M19 of $L=W=100\text{nm}$ provide for small current consumption.

Compensation design

Hand design for compensation was performed in a similar methodology to problem set 3. An initial guess for C_c was $Cl/2$, or 0.5pF. This conservative estimate provides for approximately 72 degrees of phase margin at unity gain. The gain of 2 phase margin is even better than this. This value was later adjusted in simulation to 0.4pF. R_z is constrained based on placement of the nulling resistor for the RHP zero. It is constrained in the following way, using similar arguments to problem set 3:

$$\frac{1}{g_{m_{12}}} < R_z < \frac{1}{3 * g_{m_5}}$$

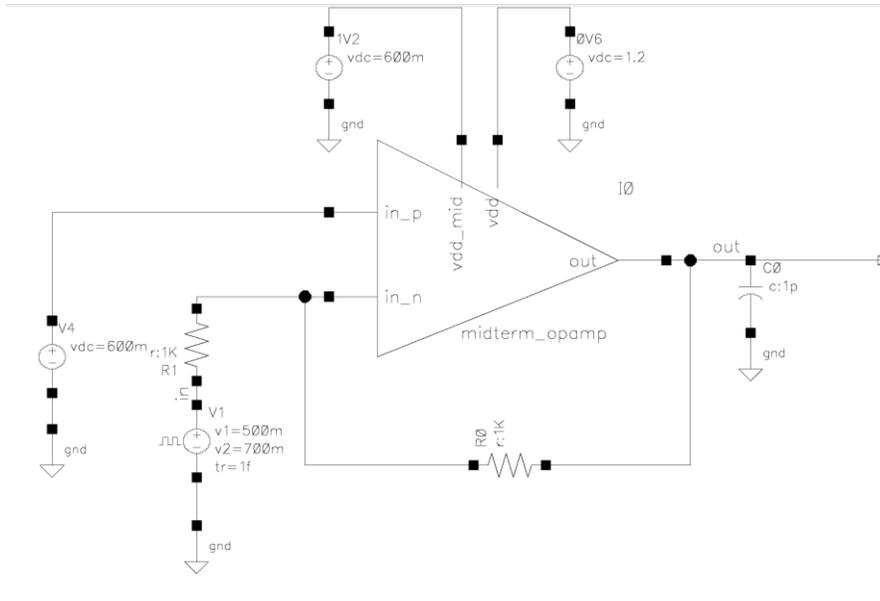
Therefore, plugging in values

$$45.6 \text{ ohm} < R_z < 121.6 \text{ ohm}$$

R_z was initially chosen to be 100 ohms. This was confirmed in simulation to be an optimal value. These hand calculations are based on the assumption that the poles are sufficiently split that the lower frequency pole dominates in phase margin.

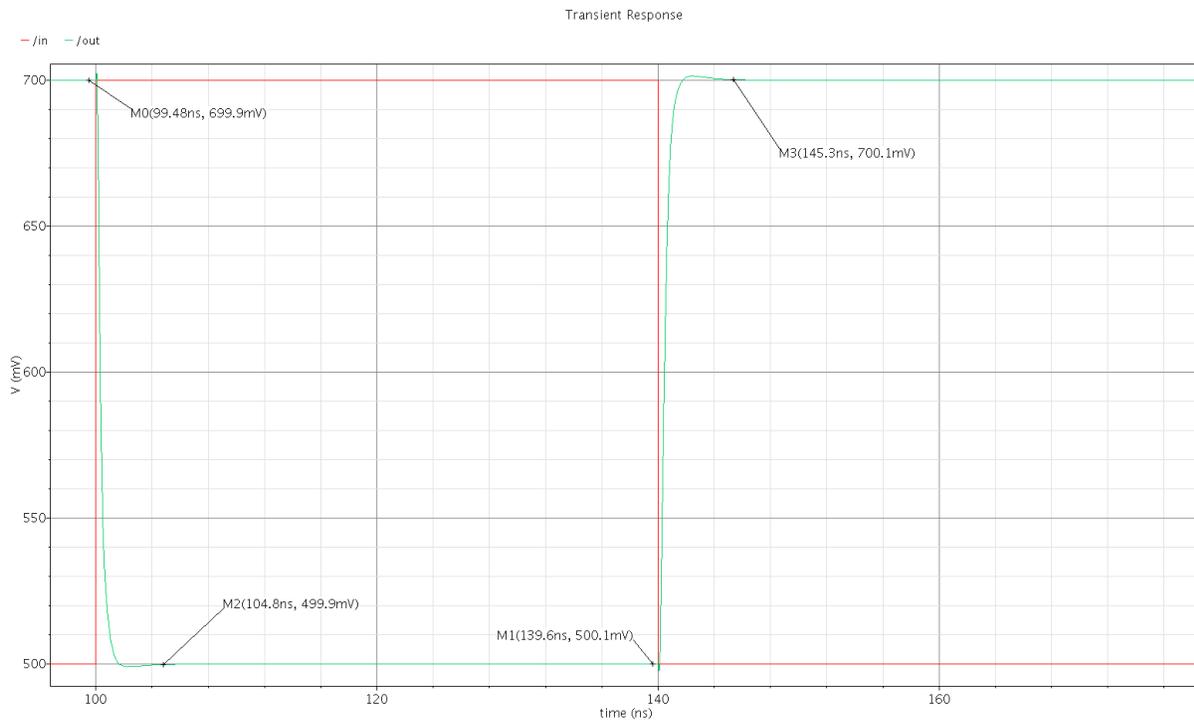
1. Settling Time

The op amp was designed with a GBW based on consideration of settling time (see calculations above). A GBW of 875MHz was chosen. With a DC gain of 5000, this results in a dominant pole of $875\text{MHz}/5000=142\text{KHz}$. Settling time was measured using the following testbench:

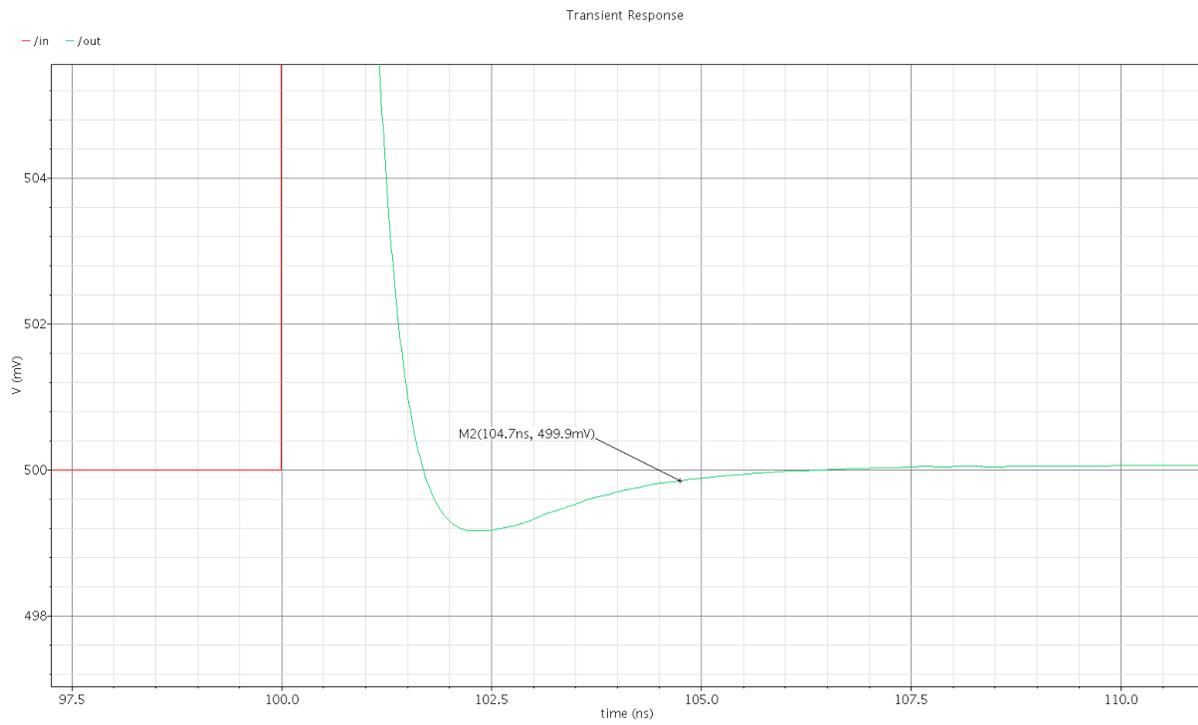


Due to minor offset, the final values are 699.9 and 500.1mV, so the 0.1% limits are 699.7-700.1mV and 499.9-500.3mV. Settling time was measured to be 5.3ns up and 4.8ns down to 0.1%. It is expected that the slew upwards is longer than the slew downwards, as the upwards slew is provided by a current source while the downwards is provided by the gain stage transistor. This was confirmed in simulation. Waveforms of the settling time are shown below.

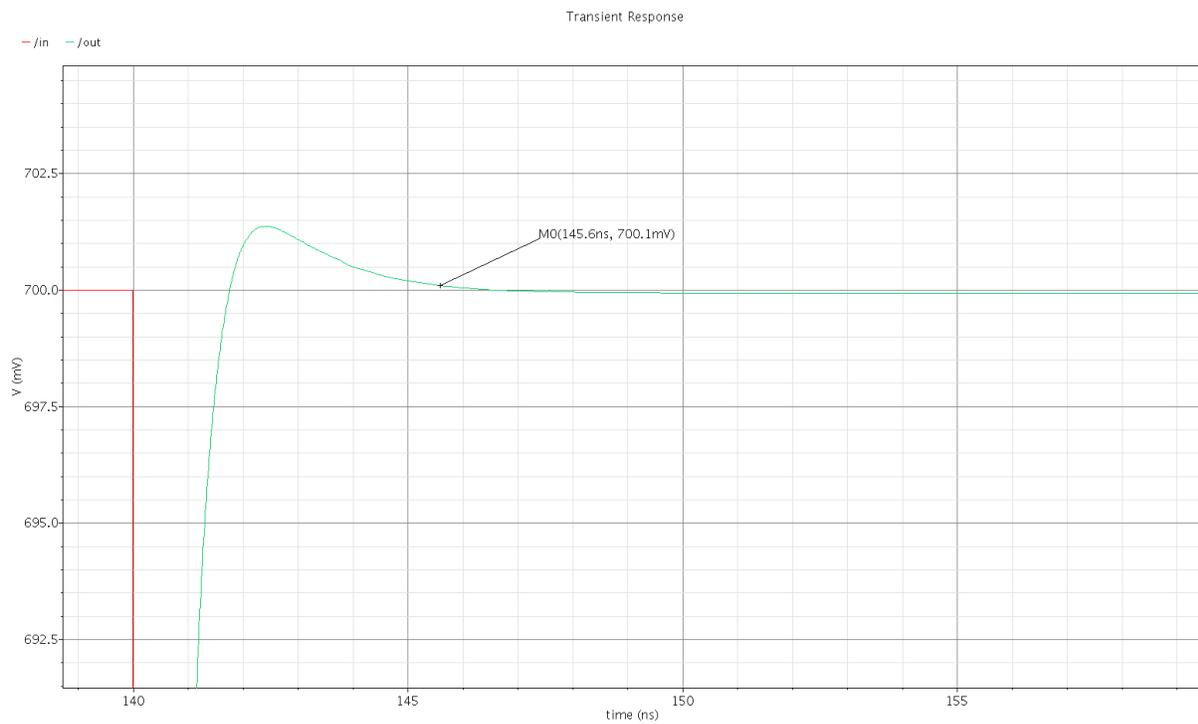
Settling time (both):



Zoomed in settling time (down)



Zoomed in settling time (up)



2. Power Consumption

Current consumption from the first stage differential pair was estimated to be $2 * 152.2\mu\text{A} = 304.4\mu\text{A}$.

Current consumption from the first stage cascade legs was estimated to be $2 * 152.2\mu\text{A} = 304.4\mu\text{A}$.

Current consumption from the second stage was estimated to be 1.216mA.

Current consumption from two current mirrors at 30uA each is 60uA.

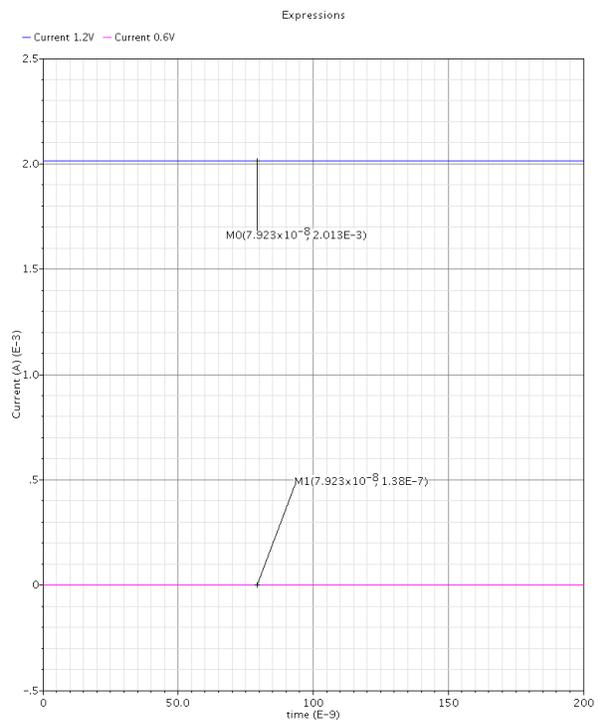
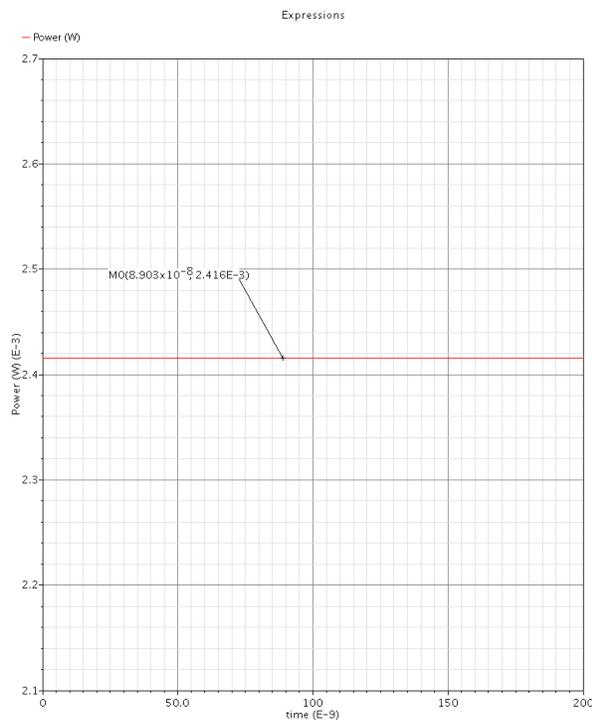
Current consumption from the bias2 voltage divider was estimated to be negligibly small.

Therefore, the estimated current consumption was estimated to be

$$(304.4\mu\text{A} + 304.4\mu\text{A} + 1216\mu\text{A} + 60\mu\text{A}) = 1884.8\mu\text{A}$$

Estimated power is then $(1.2\text{V} * 1.88\text{mA}) = 2.25\text{mW}$.

Power was measured using the same testbench as above, while holding inputs at 0.6V. As seen below, power was measured to be 2.42mW. Current consumption from the 0.6V supply was measured to be within specification at 138nA. Real current being slightly above estimates is primarily attributed to the second stage being biased at a slightly higher current density than originally calculated.



3. Output Resistance

Open-loop output resistance is the parallel combination of the output resistances of the output stage transistor and its active-load current supply:

$$R_{out} = R_{out_{M5}} \parallel R_{out_{M8}}$$

Based on OCEAN small-signal output, R_{out} of NMOS at $10\mu\text{A}/\mu\text{m} = 220\text{k}\ \Omega \cdot \mu\text{m}$.

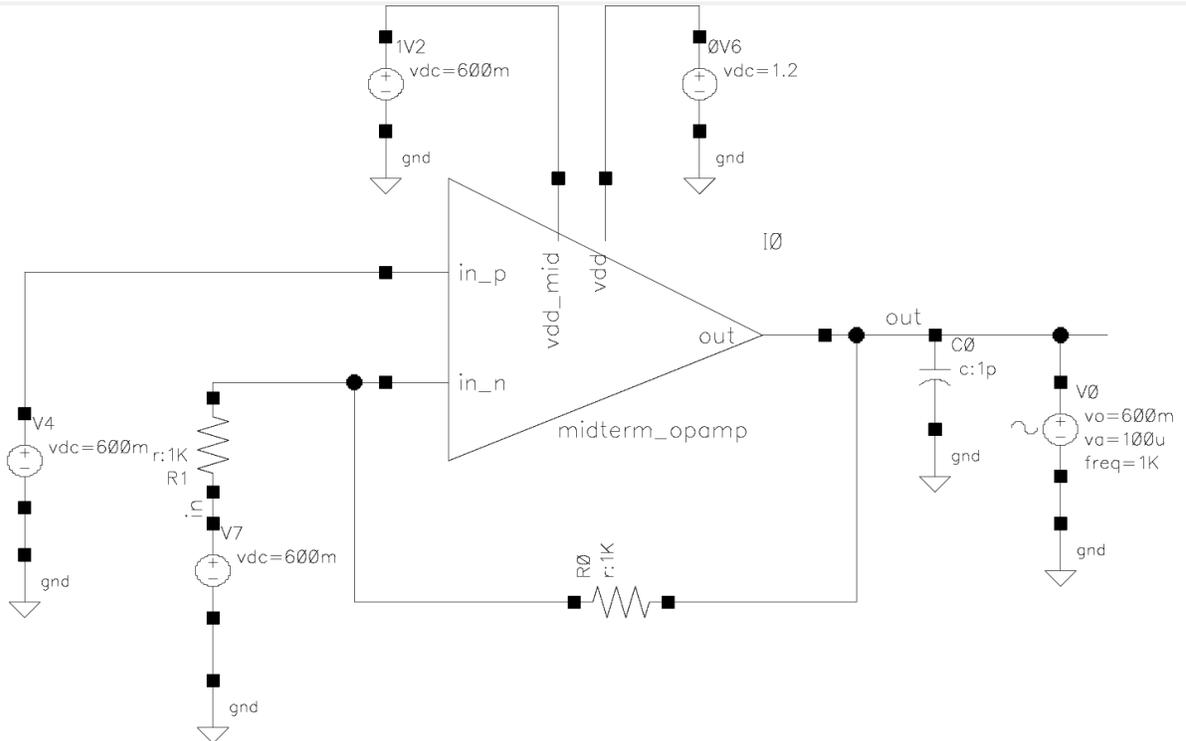
R_{out} of PMOS at $10\mu\text{A}/\mu\text{m} = 250\text{k}\ \Omega \cdot \mu\text{m}$. Therefore open loop R_{out} is estimated to be

$$R_{out_{OL_{predicted}}} = \frac{220\text{k} \cdot \mu\text{m}}{121.6\mu\text{m}} \parallel \frac{250\text{k} \cdot \mu\text{m}}{130.6\mu\text{m}} = 920\ \Omega.$$

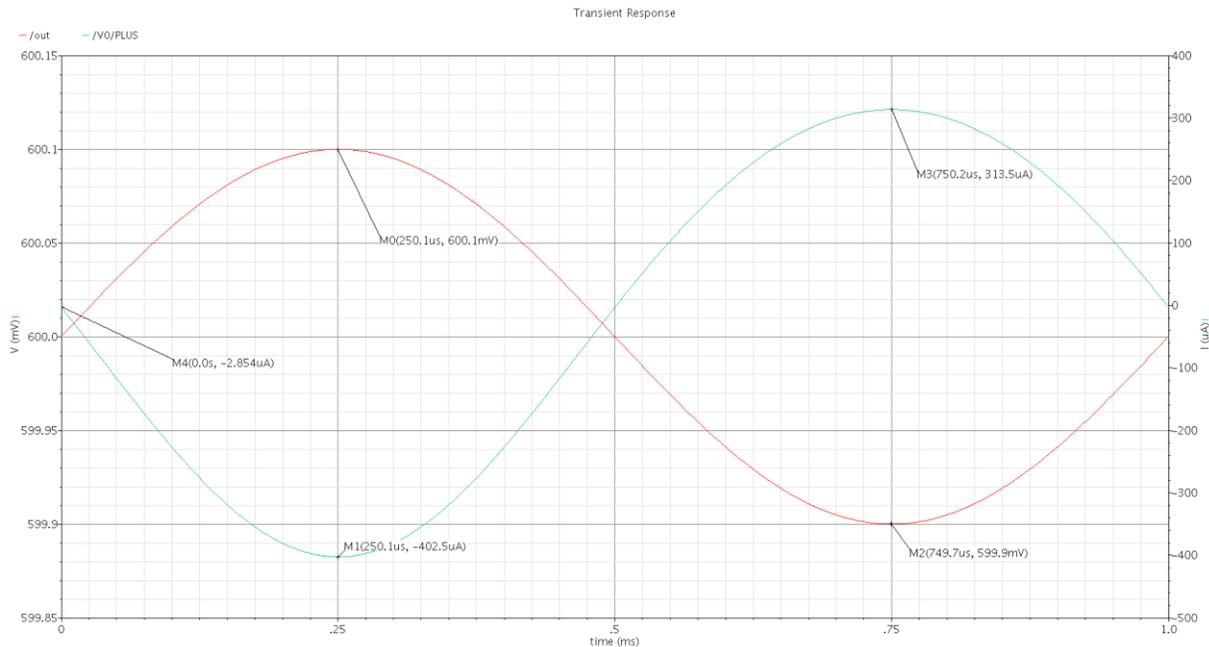
Therefore, closed loop R_{out} in a gain of 1 amplifier is predicted to be

$$R_{out_{CL_{predicted}}} = \frac{R_{out_{OL}}}{\text{Loop gain}} = \frac{920}{2500} = 368\ \text{m}\ \Omega$$

Output resistance is measured in two ways, using the following schematic testbench. After biasing the inverting amplifier at its operating point, a small-signal test voltage is applied to the output and a small-signal test current observed.



The output voltage and current waveforms are as follows:



Output resistance is measured to be

$$R_{out_{measured}} = \frac{V_{out_{pp}}}{I_{out_{pp}}} = \frac{200\mu V}{716\mu A} = 279m\ \text{ohm}$$

This is confirmed by HSPICE calculation of small-signal Gds of the two output transistors:

$$R_{out_{measured}} = \frac{1}{\text{Loop Gain} \left(\frac{1}{G_{ds_{M5}}} \parallel \frac{1}{G_{ds_{M8}}} \right)} = \frac{1865 \parallel 1683}{5000} = 176m\ \text{ohm}$$

4. Thermal Noise

For hand calculations of thermal noise, the second stage is neglected- noise is dominated by the first stage, whose noise is subjected to the gain of the entire amplifier. Input-referred noise spectral density of the first stage has been derived in the same manner as pset 4 problem 3 and is equal to (derivations omitted here for brevity):

$$\frac{\overline{V_{it}^2}}{\Delta f} = 2 * (\overline{V_{eq_{m11,12}}}^2 + \overline{V_{eq_{m9,10}}}^2 * \left(\frac{g_{m_{m9,10}}}{g_{m_{m11,12}}}\right)^2 + \overline{V_{eq_{m7,14}}}^2 * \left(\frac{g_{m_{m7,14}}}{g_{m_{m11,12}}}\right)^2)$$

Substituting in thermal noise,

$$\begin{aligned} &= 2 * \left(\frac{4kT * 3}{2 * g_{m_{m11,12}}} + \frac{4kT * 3}{2 * g_{m_{m11,12}}^2} * g_{m_{m9,10}} + \frac{4kT * 3}{2 * g_{m_{m11,12}}^2} * g_{m_{m7,14}} \right) \\ &= 2 * \left(\frac{6 * 300 * 1.3 * 10^{-23}}{.00274} + \frac{6 * 300 * 1.3 * 10^{-23}}{.00274} + \frac{6 * 300 * 1.3 * 10^{-23}}{(.00274)^2} * (30.4 * 10^{-4}) \right) \end{aligned}$$

$$\frac{\overline{V_{it}^2}}{\Delta f} = 5.29 * 10^{-17} \frac{V^2}{Hz}$$

Multiplying by bandwidth,

$$\overline{V_{it}^2} = 5.29 * 10^{-17} * 499.99 * 10^6 = 2.65 * 10^{-8} V_{rms}$$

To calculate output-referred noise, the input referred noise is multiplied by the DC gain of 6168:

$$\overline{V_{ot}^2}_{predicted} = \overline{V_{it}^2} * a_v = 2.65 * 10^{-8} * 6168 = 132uV_{rms}$$

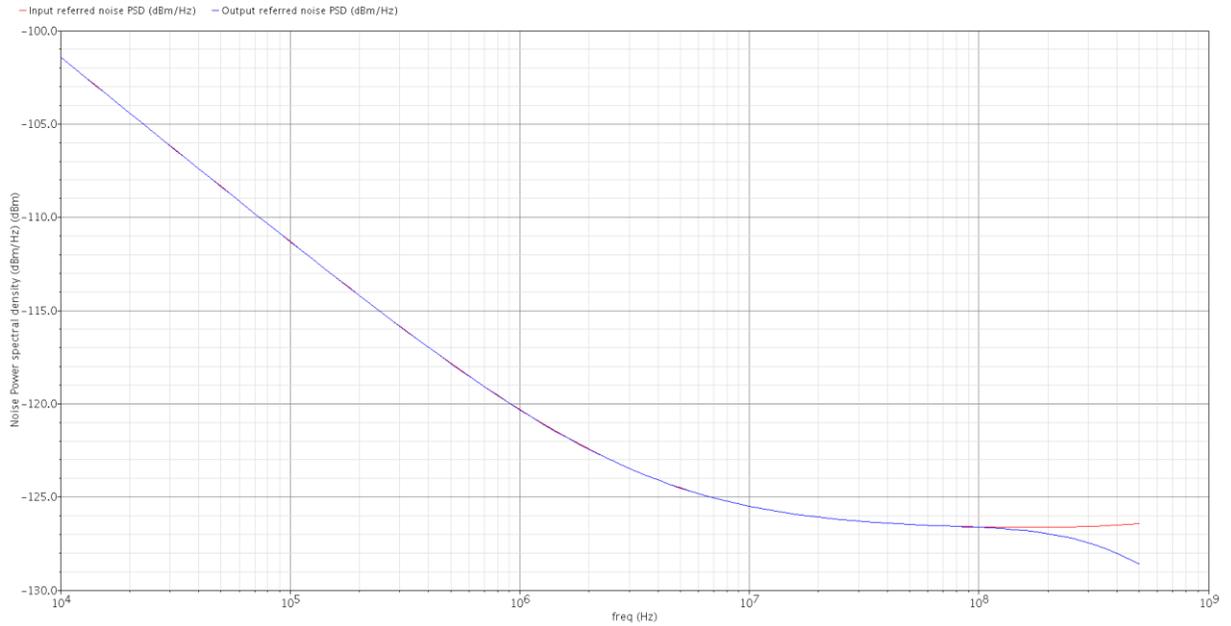
The choice to refer input noise to the output by multiplying by DC gain is not rigorous, as the amplifier's gain rolls off quickly at the first pole (140KHz), and so the gain is much lower over much of the noise integration bandwidth (up to 500MHz). However, for conservative design and ease of hand calculations the DC gain was used over the entire frequency spectrum.

Thermal noise was determined empirically using the same testbench setup as in the settling time measurement, with both inputs held at 600mV. Noise was calculated by OCEAN script, results are given below for both RMS noise and noise PSD. RMS noise over specified bandwidth was found to be 315.5uV². This value is slightly higher than was calculated in hand design as it also includes shot noise and flicker noise, which dominates at low frequencies such as in the specified bandwidth. A small part of the discrepancy may also be explained by the omission of the second stage in thermal noise calculations. As expected, the dominating noise sources are the input differential pair and the current sources in the first stage.

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ocean> load("midterm_opamp_noise_plot.ocn")
Please specify a result name.
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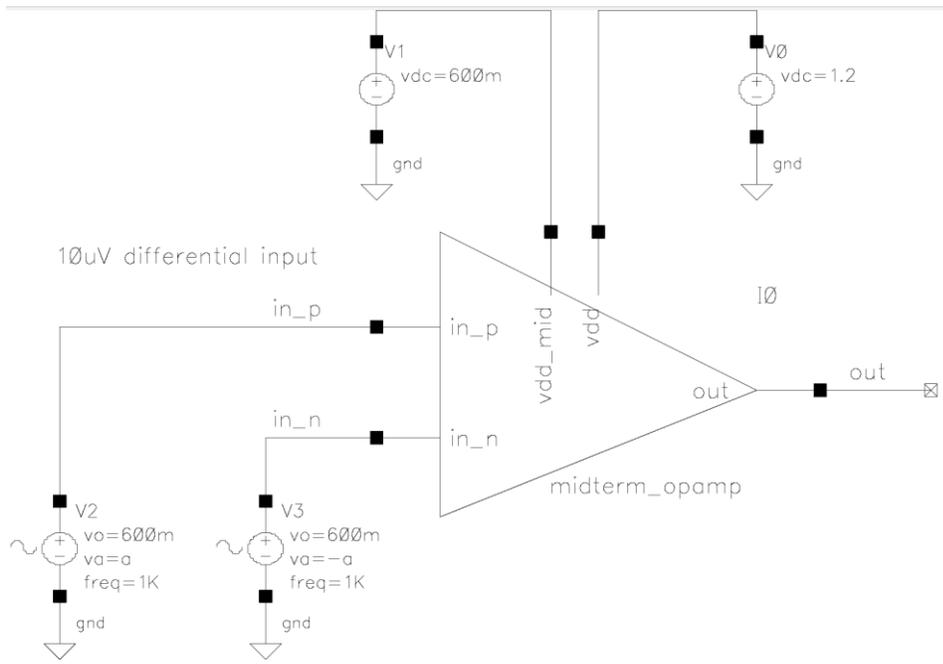
Device	Param	Noise Contribution	% Of Total
/I0/M10	id	0.000115791	13.47
/I0/M9	id	0.00011516	13.32
/I0/M11	id	0.000107823	11.68
/I0/M12	id	0.000106935	11.48
/I0/M14	id	9.77576e-05	9.60

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Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000315548
Total Input Referred Noise = 0.000340848
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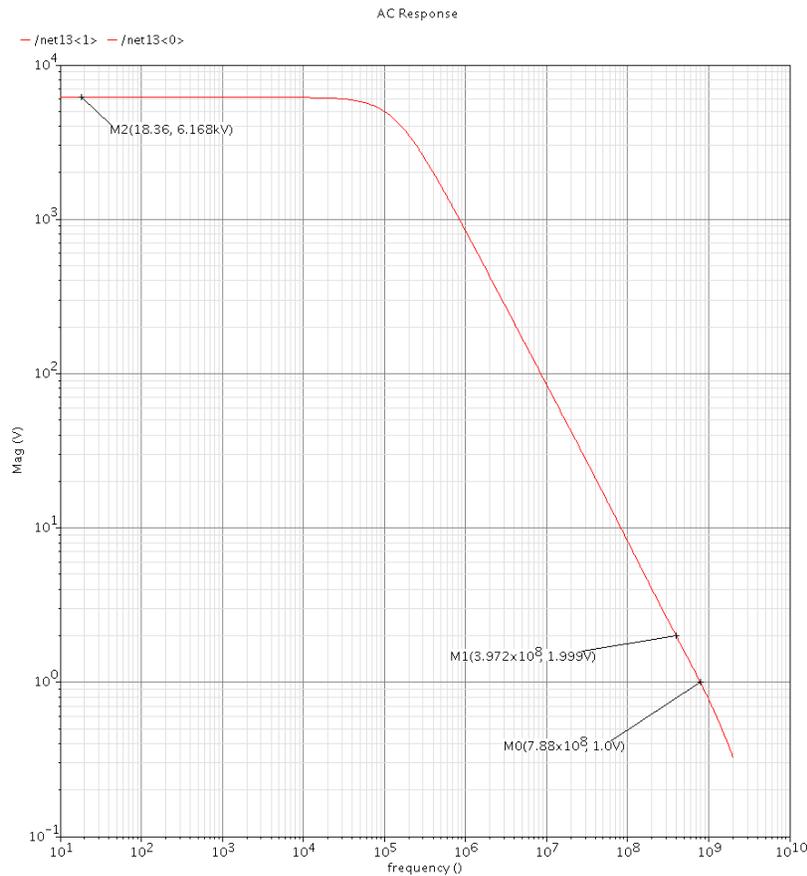


5. Small Signal Gain

Small signal gain was determined by design, as calculated above. Based on a specified gain of 5000, a gain of 6000 was chosen for margin. The open-loop gain was measured using the test circuit below.

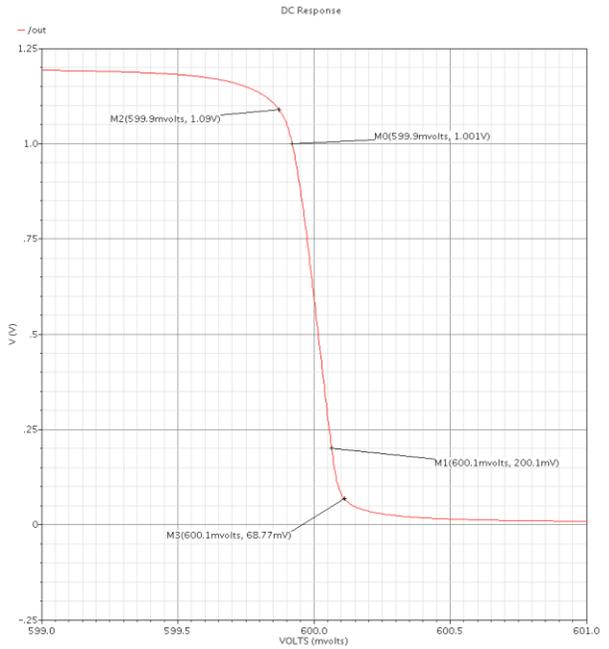
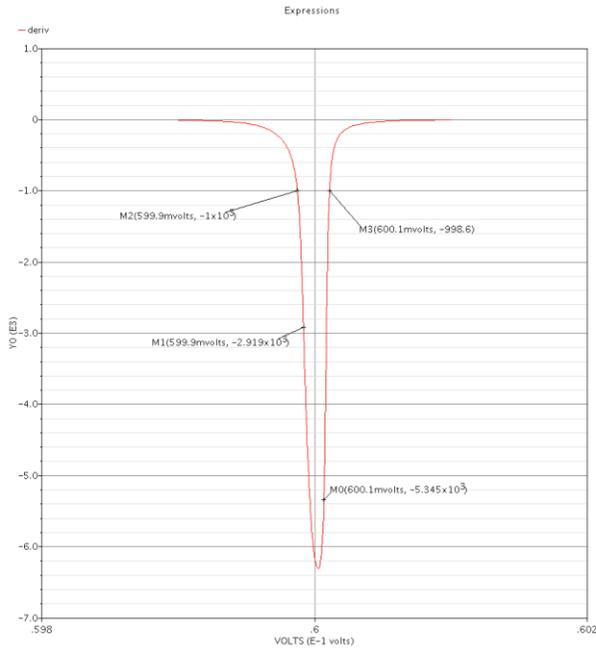


Gain was measured to be 6168 at DC:



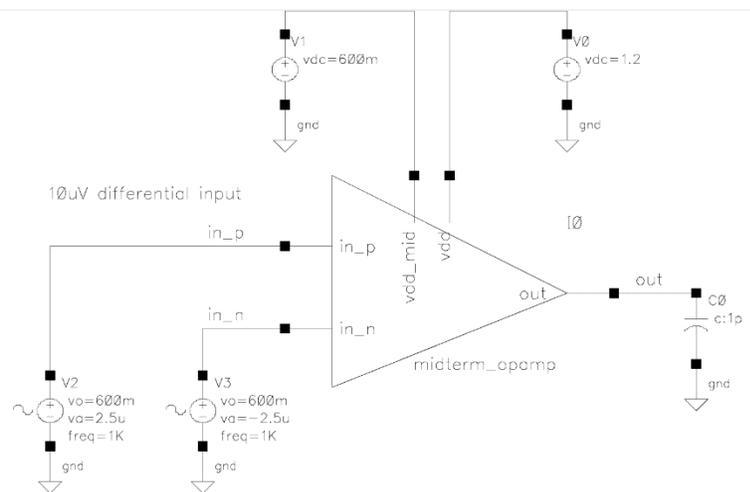
6. Output Swing

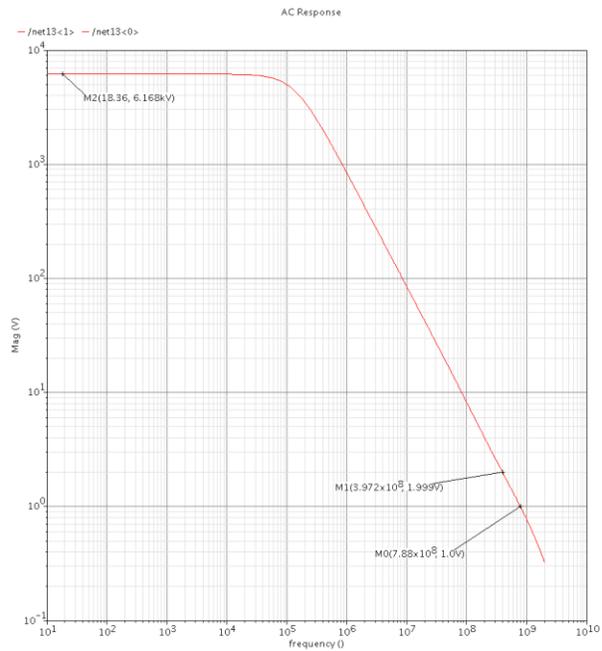
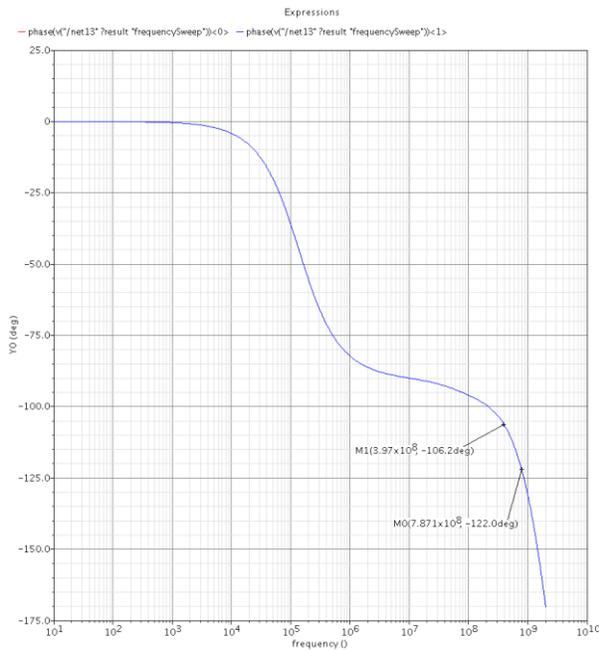
Due to the gain of the second stage, the output transistors will saturate before transistors in the first stage. Therefore, output swing in this topology is largely determined by $V_{ds,sat}$ of the output stage transistors. This is 62mV and 150mV for the NMOS and PMOS, respectively. Therefore, in a first-order hand approximation the output swing will be from 62mV to (1200-150)=1050mV. The testbench used is the same as that used in DC gain measurement, with no load. The noninverting input was held at 600mV, while the inverting input was swept in a DC analysis from 599mV-601mV, while observing the output voltage (see below, right waveform). By differentiating the output voltage, it is possible to determine the gain as a function of output voltage (see below, left waveform). As seen below, at 0.2V and 1.0V the gain of 1000 requirement is easily met, with the real gains being 2919 and 5345, respectively. The gain of 1000 crossover occurs at 68mV and 1090mV, well within specification and aligning well with the hand estimation. The output stage was biased at a slightly higher current than was calculated in hand design (1.21mA for hand calculation vs 1.36mA in simulation). The increased V_{dsat} associated with this increased current density likely explains the worse output swing performance than was predicted.



7. Phase Margin

Phase margin was predicted to be 72° by design (see above). Phase margin was measured in an open-loop configuration with 1pF load (see below). A small signal differential input was applied, and output phase observed. Phase margin was found to be 58° at unity gain and 73.8° at a gain of 2 crossover. The design was based on a 72° phase margin at unity gain. The true unity gain phase margin is much worse than this due to the pole associated with the large parasitic capacitance and large output resistance of the first stage, as a consequence of the cascode topology. The phase margin at gain of 2 crossover is an improvement from hand calculations because the hand calculations were based on phase margin at unity gain, and measured phase margin is better at gain of 2 crossover because it occurs at a lower frequency.





8. PSRR

As derived in lecture, PSRR stems from two root causes. The first is ripple on the power supply coupling through the PMOS current sources in the first stage and appearing analogously to a common-mode input. This impact is identical to that of a common mode input (see below for CMRR calculation)

$$a_{+1} = -a_{vc1}a_2 = -0.39$$

The second cause for PSRR is ripple on the positive rail seen through the voltage divider of the output stage. Therefore,

$$a_{+2} = \frac{r_{o5}}{r_{o5} + r_{o8}} = \frac{1800}{1800 + 1920} = 0.48$$

This occurs in the opposite polarity of the first stage's PSRR impact, so some beneficial cancellation of PSRR occurs. The total power supply gain is the sum of these two individual gain contributions, $a_+ = 0.48 - 0.39 = 0.09$. Therefore, the predicted PSRR at DC is equal to

$$PSRR_{+predicted} = -20 \log\left(\frac{a_{vd}}{a_+}\right) = -20 \log\left(\frac{6168}{0.09}\right) = 97dB$$

At 50KHz, capacitive effects are negligible, so a_+ is largely unchanged. The dominant pole is at 140KHz, so the differential gain is largely unchanged as well. Therefore, the predicted PSRR at 50KHz is well approximated by the PSRR at DC.

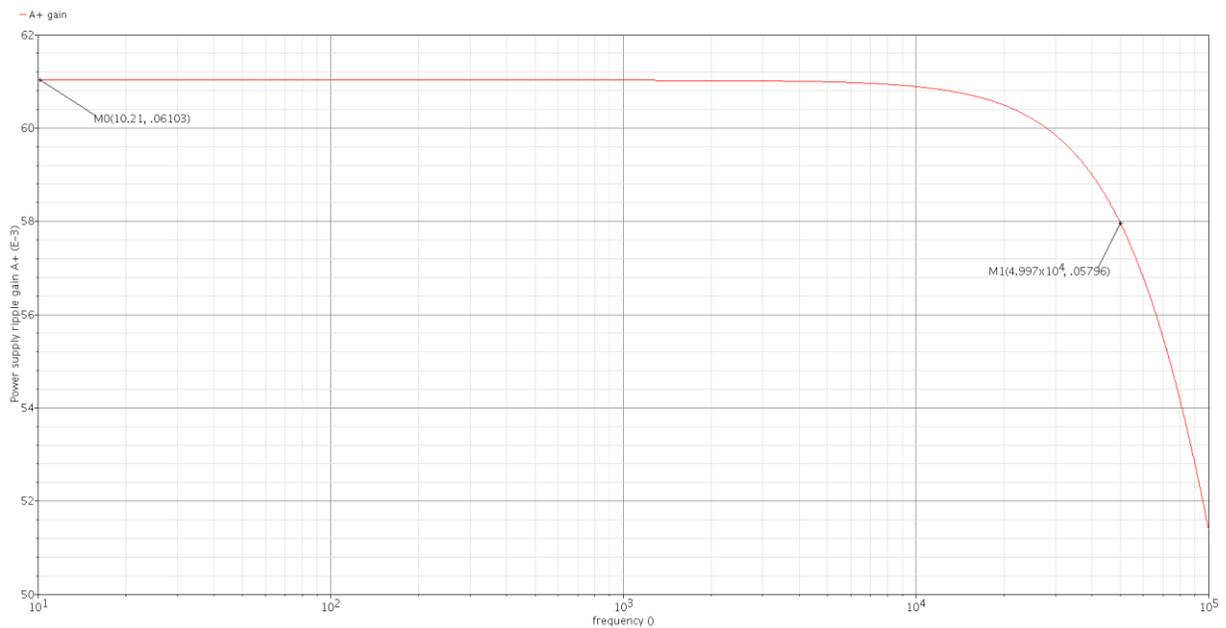
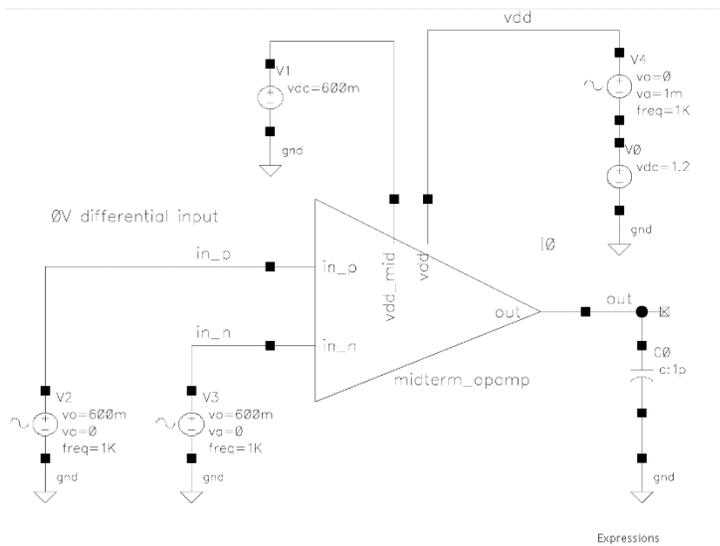
PSRR was measured by applying a small signal voltage on the positive supply, VDD (see below) in an AC analysis. The gain from vdd to output, A+, is defined as the amplitude ratio of vdd and the output node:

$$A_+ = \frac{|output|}{|vdd|}$$

PSRR is defined as the gain ratio between the differential gain and vdd gain, and the measured values are:

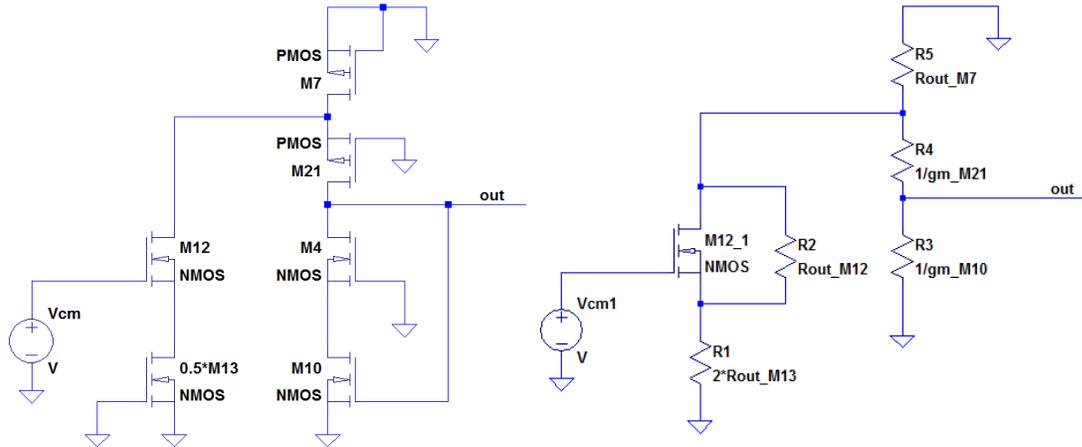
$$PSRR_{measured} = -20 \log_{10} \left(\frac{A_{vd}}{A_+} \right) = -20 \log_{10} \left(\frac{0.061}{6168} \right) = 100.1dB \text{ (at DC)}$$

$$= -20 \log_{10} \left(\frac{0.0579}{5800} \right) = 100.0dB \text{ (at 50KHz)}$$



9. CMRR

For CMRR hand analysis, the input stage was divided into a half-circuit, as seen below (left). It further simplifies as seen on the right.



Plugging in numbers and iterating KCL on the drain of M12, the gain from common mode input to output of the first stage is found to be 0.022. Multiplying by the gain of the second stage, the total common mode gain is

$$a_{vc} = a_{vc_stage1} * a_{v_stage2} = 0.022 * 18 = 0.39$$

Therefore, the CMRR is predicted to be the following:

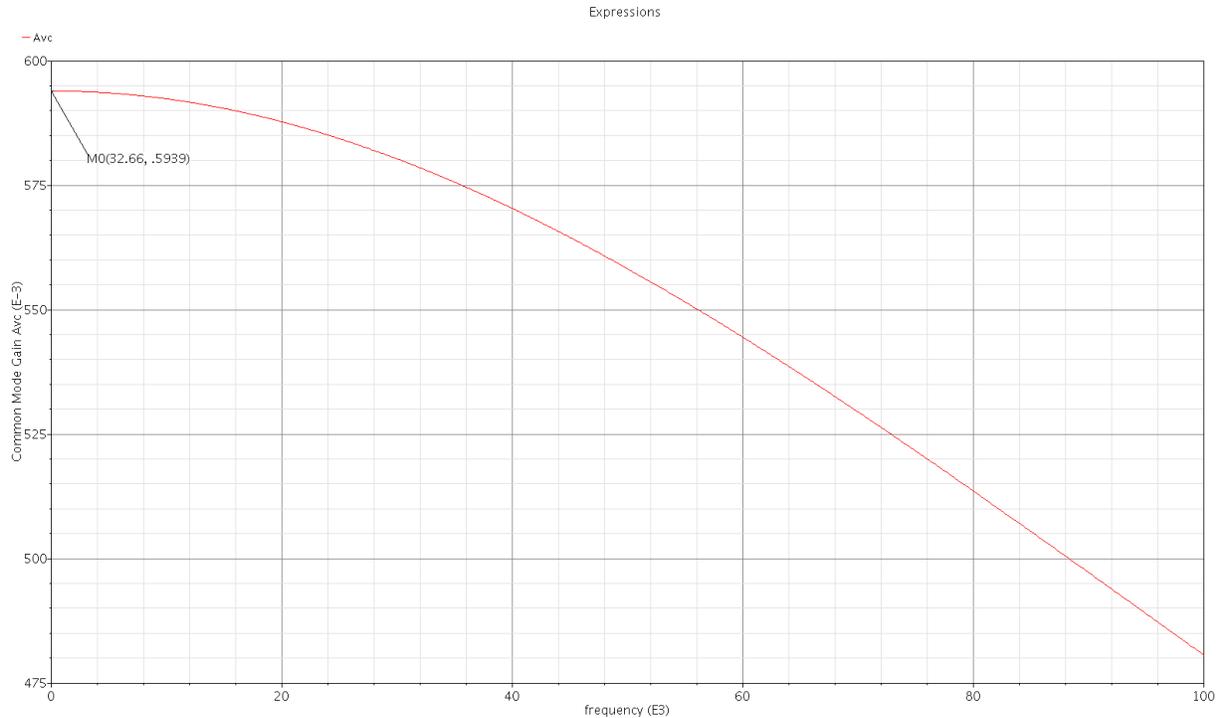
$$CMRR_{predicted} = -20 \log_{10} \left(\frac{a_{vd}}{a_{vc}} \right) = -20 \log_{10} \left(\frac{0.39}{6168} \right) = 83dB$$

Common mode rejection ratio was measured using the same test circuit as in PSRR (see above, PSRR section). A common-mode input voltage was applied in an AC analysis (around Vcm=600mV) and small-signal output amplitude observed. The common mode gain is defined as the amplitude ratios of the common mode input and the output:

$$A_{vc} = \frac{|output|}{|CM\ input|}$$

The common mode rejection ratio is defined as the gain ratio of the common and differential modes and was measured to be

$$CMRR_{measured} = -20 \log_{10} \left(\frac{A_{vd}}{A_{vc}} \right) = -20 \log_{10} \left(\frac{0.5939}{6168} \right) = 80.3dB\ (at\ DC)$$



Discussion

There were many tradeoffs inherent in this design, as many design variables and specifications are interconnected. The choice of a folded cascade-common source amplifier allowed for large gain and output swing while still fitting within the low voltage power supply. The FC-CS topology has a downside of high power consumption, making the power consumption specification a challenge. In addition, the high output resistance of the first stage increases noise over many other topologies, forcing wider transistors and more current in the first stage to compensate and meet specification. The high internal parasitic capacitance and output resistance associated with the first stage negatively impacts frequency response and phase margin. Fortunately, despite this it was possible to meet the settling time specification with good stability.

The choice of compensation capacitor and resistor, chosen for unity-gain stability, resulted in an excessively conservative phase margin of 74° at a gain of 2 crossover. This is also seen in the step response, which is overdamped and approaching that of a first order system (90° phase margin). While settling time specifications were met, settling time could have been improved by altering compensation to reduce phase margin while still remaining stable.

The design gain of 6000 was somewhat excessive and could be reduced to save area/cost by reducing device length. This would come at the cost of PSRR and CMRR (both well above specification) while simultaneously reducing v_{dsat} (improving output swing) and reducing output resistance.

The biasing structure for the cascade transistors could have been optimized. The $\frac{1}{2}$ voltage divider on the mid-rail supply could have instead been implemented as a $\frac{1}{4}$ divider from vdd, reducing the need for the mid-rail supply in the circuit, thus reducing interconnect cost and complexity. In addition, the decision to derive the bias from the mid-rail supply makes the circuit sensitive to noise on the mid-rail supply in addition to the power supply. This was not given in the specifications but could be an issue in a real system. In addition, both the voltage divider scheme for generating bias2 and the diode-connected transistor for generating bias3 are sensitive to process variation, and a better bias scheme could be used in future iterations. Despite these possible improvements, a successful design was implemented which meets the required specifications.