Nathan Monroe

monroe@mit.edu

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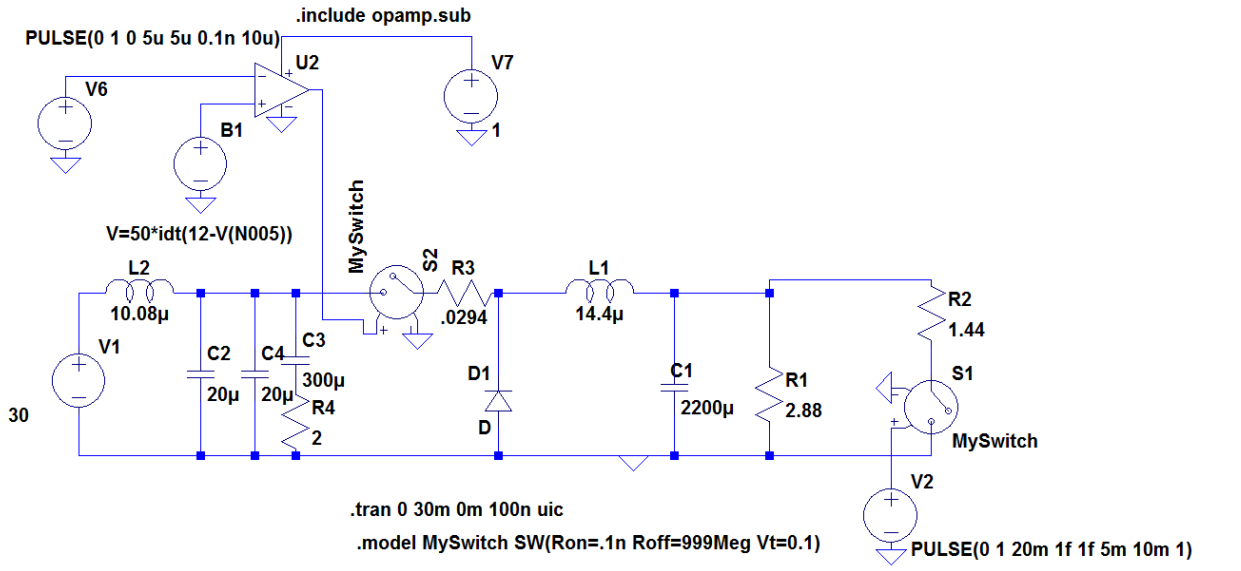
6.334 Final Project – Buck Converter

Design

Input Filter	Filter Capacitor - 40µF – 2x 20µF Capstick CS6 film capacitors in parallel
	Filter Inductor - 10.08µH – RM10/I-3F3-A630 Core with 4 windings of AWG-9
	Damping Leg - R-C Parallel with R=2Ω and C= 330µF Nichicon Aluminum Electrolytic HD
Power Stage	MOSFET- IRFZ48N
	MOSFET Heat Sink – Redtherm 6098B, R_θ=14.0 $^0C/W$
	Diode – IR30CPQ045
	Diode Heat sink - Redtherm ML26AA, R_θ=17.9 $^0C/W$
	Switching Frequency – 100kHz
Output Filter	Filter Inductor – 14.4µH – RM12/I-3F3-A40 Core with 6 windings of AWG-8
	Filter Capacitor - 2200µF U767D 35V United Chemi-Con Aluminum Electrolytic
Feedback	Transfer Function: $\frac{d}{e}(s) = \frac{50}{s}$
	Where e(s) is the laplace transform of the output error, (12-V_{out})

	Specified	Calculated	Simulated
Input Voltage Range	20 V to 30 V	20 V to 30 V	20 V to 30 V
Input Voltage Transient Limit	44V for up to 1ms	Met	N/A
Output Power Range	50 W to 150 W	50W to 150W	50 W to 150W
Output Voltage (Static)	12V ± 3%	N/A	Met
Output Voltage (Transient Limit)	12V ±20%	N/A	Met
Output Voltage Ripple, peak-peak	100mV	67.2mV ± 21.7mV	67.0mV
Input Current Ripple, peak-peak	100mA	100mA	99mA
Efficiency	85%	94%	N/A
Ambient Temperature Range	-20^{0}C to +50^{0}C	Met	N/A



Switching Frequency

Switching frequency was chosen first as a starting point for other calculations. 100KHz was chosen for multiple reasons. First, with a low switching frequency, most harmonic content is at low frequencies, reducing issues with EMI. Next, at lower frequencies certain parasitics can be neglected, such as ESL of the capacitors. Finally, at a low switching frequency switching losses are lower.

Output Filter Design

Output filter was designed to meet 0.1V output voltage ripple specification. Output voltage is the result of the output capacitor filter integrating inductor ripple current, plus a contribution from capacitor ESR. Inductor ripple current is in turn an integral of switching voltage ripple from the power stage. As calculated in Pset 3.1b, V_{pp} on the capacitor is equal to the following:

$$Vc_{pp} = \frac{I_{lpp} * D * T}{4 * C}$$

In the worst case scenario, Vin = 30V, and D = 0.6. From 100KHz switching frequency, T=10µs. Since the ripple current through the inductor is assumed to go through the capacitor, it also goes through the capacitor's equivalent series resistance. The contribution from ESR is:

$$Vr_{pp} = I_{lpp} * ESR$$

Inductor ripple current is caused by the inductor integrating the voltage difference $V_{in} - V_{out}$, with the maximum value at time DT in the cycle:

$$\Delta Il_{pp} = \frac{(V_{in} - V_{out})DT}{L}$$

Since the capacitor is in series with it's ESR and in parallel with the load resistor, and substituting Il_{pp} the output voltage is given by:

$$V_{pp} = \frac{(V_{in} - V_{out})DT}{L}(ESR + \frac{DT}{4C})$$

The worst-case scenario is V_{in} = 30V and D=0.4. Inductor sizing and Capacitor model and sizing (accounting for ESR) were chosen to meet the constraint of V_{pp} < 0.1V. This results in the following constraint on L, C, and ESR:

$$L \geq 7.2 * 10^{-4}(ESR + \frac{10^{-6}}{C})$$

To keep inductor size reasonable, a large capacitor was chosen. The choice made was the United Chemi-Con U767D aluminum electrolytic capacitor, rated at 35V (with 44V surge) and 2200µF. Plugging into the equation, this results in a minimum inductor size of 12.49µH. The chosen value was 14.4 µH. This results in a calculated V_{pp} of 0.67mV, which is matched closely by simulation. The capacitor has a ±30% tolerance in ESR, which translates to variability in output ripple voltage of ±21mV. Even in the worst-case scenario for ESR tolerance and input voltage, the output ripple voltage is still within specification.

The capacitor's maximum ripple current specification of 10.01A is easily met, with the actual ripple current being approximately 1.44A RMS.

Output filter inductor design

The output filter was designed with the following constraints in mind:

- $B_{max} < 0.3T$
- Windings fitting within winding area of core
- Windings carrying no more than $500A/cm^2$
- Minimum L = 12.5µH
- Minimizing power loss

As in pset problems, $Il_{pp} = \frac{DT(V_{out}-V_{in})}{L}$. In the worst case, with V_{in} = 30V and D=0.4, $\Delta Il_{pp} = 5A$. Thus, maximum current is ($I_{out} + \frac{\Delta Il_{pp}}{2}$). At the worst case of 150W output, this is (150/12) + 2.5 = 15 Amperes. The constraint on $B_{max} < 0.3T$ results in the following constraint:

$$N \geq \frac{L * Il_{MAX}}{A_E B_{MAX}}$$

L, Il_{MAX}, and B_{MAX} are known. A_E is known for each inductor core. The constraint on minimum number of turns is calculated for each core and tabulated below.

The constraint on winding current density places a constraint on winding wire gauge, according to the following:

$$\frac{15A}{area} \leq \frac{500A}{1cm^2}$$

This yields a minimum winding area of 0.030 cm^2, or a diameter of 1.95mm, translating to AWG-12 copper wire.

A further constraint comes from the fact that the windings must physically fit in the winding area of the core, accounting for a packing factor of approximately 0.5. This yields the following equation:

$$\frac{A_{Winding}}{2} = N * \pi * (\frac{D}{2})^2$$

This places a constraint on the maximum number of windings for each inductor core. Winding area for each core was calculated from the physical dimensions, obtained in the datasheet. The winding area constraint for each core is tabulated below.

The table below shows the results of the above constraints over core and wire gauge. When conflicting constraints cause a core/gauge combination to be impossible, it is colored in red. Otherwise it is colored green.

	B < 0.3T constraint	AWG8 A_{wind} constraint	AWG9 A_{wind} constraint	AWG10 A_{wind} constraint	AWG11 A_{wind} constraint	AWG12 A_{wind} constraint
RM8: $A_e = 63mm^2$	N ≥ 12	N ≤ 2	N ≤ 3	N ≤ 4	N ≤ 5	N ≤ 7

A_w=45.63mm^2						
RM10: A_e = 96.6mm^2 A_w=63.86mm^2	N ≥ 8	N ≤ 3	N ≤ 4	N ≤ 6	N ≤ 7	N ≤ 9
RM12: A_e = 146mm^2 A_w=102.5mm^2	N ≥ 5	N ≤ 6	N ≤ 7	N ≤ 9	N ≤ 12	N ≤ 15
RM14: A_e = 198mm^2 A_w=145.6mm^2	N ≥ 4	N ≤ 8	N ≤ 10	N ≤ 13	N ≤ 17	N ≤ 22

The cells colored green represent choices of wire gauge and core which meet constraints for wire current density, core flux density, and winding area. From these options, decisions were made to match inductor size constraints while minimizing power consumption. Due to the relatively low switching frequency, skin effect was neglected and it was assumed that resistive losses would dominate over core losses. Thus, the RM12-A400 core was chosen with 6 windings of AWG8. This results in an inductance of 6^2* 400nH = 14.4μH. Confirming that the B_{max} constraint is met:

$$B_{MAX} = \frac{L * I_{MAX}}{N * A_E} = 0.246T$$

Inductor loss is due to contributions from conduction loss and core loss. Conduction loss is equal to

$$P = I_{RMS}^2 * \frac{Resistance}{Km} * N * L_{TURN}$$

where resistance/Km was found for AWG8 from the Verghese et al textbook table 20.1. This equation simplifies to $P = I^2R$. The calculated resistive power loss is

$$P = (\frac{150W}{12V})^2 * \frac{2.51\Omega}{Km} * 6 * 61 * 10^{-6}Km = 0.143W$$

Core loss is equal to:

$$P_{CORE} = C_m * F^{\alpha} * (B_{AC,PK})^{\beta} * V_{CORE} = 2.5 * 10^{-4} * (100{,}000)^{1.63} * (0.082)^{2.45} * 8.34 = 642.6mW$$

where the coefficients were found from the design project handout, Vcore from the data sheet. $B_{AC,PK}$ was calculated according to the following:

$$B_{AC,PK} = \frac{L * \Delta I_{lpp}}{N * A_e} = \frac{14.4 * 10^{-6}\mu H * 5A}{6 * 146mm^2} = 0.082T$$

Thus, total inductor loss is 0.143 + 0.642 = 0.7856W. In terms of thermal constraints, core temperature is equal to the following:

$$T_{core} = T_{Amb} + R_{\theta} * P_{diss} = 50 + 0.7856 * 23 = 68.06\ ^{0}C$$

This is within the maximum temperature of 90C for 3F3 material.

Power MOSFET Selection

Power device selection was based on minimizing power dissipation while meeting constraints for voltage blocking and current conduction. For a power MOSFET, total loss is due to switching loss and conduction loss:

$$P = P_{SW} + P_{COND} = I_{AV}^2 * R_{ON} * D + 0.5 * V_{IN} * \left(\frac{P_{out}}{V_{out}}\right)(T_f + T_r) * F_{SW}$$

$$= (\frac{150}{12})^2 * 0.4 * R_{ON} + 0.5 * 30 * \frac{150}{12}(T_f + T_r) * 100{,}000$$

This is based on the assumption that due to low switching frequency and MOSFET gate capacitance, capacitive losses can be neglected. The results for each MOSFET choice are tabulated below, assuming worst case Pout = 150W, Vin = 30V, D = 0.4, and T = 150^{0}C. The temperature affects on-state resistance according to the device datasheets.

	Ron (mΩ)	T_f+T_r (ns)	P_{total}(W)
IRFZ24N	0.07*2	61	9.89
IRFZ34N	0.04*1.85	89	6.29
IRFZ44N	0.0175*2.1	105	4.265
IRFZ48N	0.014*2.1	128	4.237
IRL2505N	0.008*2	224	5.575

Larger switching devices have a lower on resistance, reducing conduction losses, but they also have a high gate capacitance, increasing rise/fall time and thus switching losses. The optimum device for power efficiency is the IRF Z48N, which is the device that was selected. In addition, the Z48N meets all specifications for conducted current and blocked voltage under worst-case conditions.

MOSFET Heat Sink Selection

The thermal model of the MOSFET consisted of a current source of value P_{diss}, in series with three resistors, with thermal resistance $R_{\theta JC}$ for the thermal resistance between junction and case, $R_{\theta CS}$ for the thermal resistance between case and heatsink, and $R_{\theta SA}$ for the thermal resistance between sink and ambient. Junction temperature has the constraint of a maximum of 150C. In the worst case ambient temperature of 50C and power dissipation of 4.23W, junction temperature is given by the following:

$$T_{JMAX} = T_A + P_{DISS} * (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) = 50 + 4.23(1.15 + 0.5 + R_{\theta SA})$$

Thus, the maximum sink to ambient thermal resistance is 17.7 C/W. The Redtherm 6098B heatsink was chosen, with $R_{\theta SA}$ = 14.0 C/W. This provides adequate heat dissipation to keep Tj under 150C, and also fits the TO-200 MOSFET package. In this case the maximum junction temperature is 116.3C.

Power Diode Selection

Power diode was selected based on minimizing power loss, while meeting blocked voltage and conducted current specifications. Neglecting reverse-recovery loss, diode loss is due to forward voltage drop during conduction:

$$P = I_{RMS} * V_{FW} = (1 - D) * \left(\frac{P_{MAX}}{V_{OUT}}\right) * V_{FW} = 0.6\left(\frac{150}{12}\right) * V_{FW}$$

This is assuming worst-case conditions, P = 150W and D = 0.4. The results for each diode are tabulated below, using V_{fw}, forward voltage drop, at worst-case T_j of 150C.

	V_{fw} (V)	Power Loss (W)	Meets current spec?
MBR340	0.9	6.75	No
IRF6TQ	0.65	4.875	No
IRF10TQ	0.6	4.5	No
IRF18TQ	0.5	3.75	Yes
IRF30CPQ	0.5	3.75	Yes

As shown by the table, the IRF18TQ and the IRF30CPQ have roughly the same power dissipation, and are the only two diodes which meet the conducted current specification. The IRF30CPQ was chosen because of slightly better thermal performance over the IRF18TQ.

Diode Heat Sink Selection

The diode heat sink was chosen in the exact same manner as described for the power MOSFET. For the diode, T_{jmax} = 125C, $R_{\theta JC}$=1.1 C/W, $R_{\theta CS}$=0.24 C/W. It was calculated that to meet T_j constraints, $R_{\theta SA}$ must be less than 18.66 C/W. The Redtherm ML26AA was chosen, with $R_{\theta SA}$=17.9 C/W. The maximum worst-case T_j = 122.19C.

Input Filter Design

The input filter was designed to meet the input ripple current specification. This was implemented as a second order LC low pass filter. The worst case unfiltered input current is approximately a square wave of frequency equal to F_{sw}, and amplitude equal to (Pout/Vout) = 150/12. Most energy is contained in the fundamental frequency of this signal, which has a frequency of 100KHz and an amplitude of

$(4/\pi)*(150/12) = 15.9A$. The desired amplitude is 0.1A, requiring a gain of 0.1/15.9, or 0.0063 = -44dB. A second order filter has frequency response of -40dB/decade above the cutoff frequency, so a cutoff frequency of ~9500Hz is necessary. This translates to $LC = 2.8*10^{-10}FH$. An inductance of 10.08µH was chosen, requiring a minimum capacitance of 27.7µF. Two 20µF capstick CS4 film capacitors were chosen in parallel, to give a total capacitance of 40µF. The maximum RMS current specification of 16.7A for the capacitors is easily met. Calculated Ipp = 100mA.

An R-C parallel damping leg was added to damp the filter response at resonant frequency. To obtain less than 10dB of peaking, a resistance of 2Ω was chosen. This satisfies the current transfer function at the resonant frequency:

$$\left|\frac{Iy}{Ix}\right| = \frac{R_D}{\sqrt{\frac{Lf}{Cf}}}$$

Damping capacitor was chosen to be sufficiently larger than filter capacitor, so a 330µF HD series Aluminum Electrolytic capacitor was chosen. The I_{rms} falls well within specification for this capacitor.

Input Filter Inductor Design

Input filter inductor was selected using the same methodology as the output filter inductor, resulting in the following table:

	B < 0.3T constraint	AWG7 A_{wind} constraint	AWG8 A_{wind} constraint	AWG9 A_{wind} constraint	AWG10 A_{wind} constraint	AWG11 A_{wind} constraint	AWG12 A_{wind} constraint
RM8: $A_e = 63mm^2$ $A_w=45.63mm^2$	N ≥ 4	N ≤ 2	N ≤ 2	N ≤ 3	N ≤ 4	N ≤ 5	N ≤ 7
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RM12: $A_e = 146mm^2$ $A_w=102.5mm^2$	N ≥ 2	N ≤ 5	N ≤ 6	N ≤ 7	N ≤ 9	N ≤ 12	N ≤ 15
RM14: $A_e = 198mm^2$ $A_w=145.6mm^2$	N ≥ 2	N ≤ 6	N ≤ 8	N ≤ 10	N ≤ 13	N ≤ 17	N ≤ 22

The RM10-630 core was chosen with A_l = 630nH and four windings of AWG9, resulting in a total inductance of 10.08µH. This minimized losses while still meeting constraints. B_{max} was calculated to be 0.299T. Core losses were calculated as described above, resulting in a conduction loss of 0.0369W, and a

core loss of 0.0554W, for a total loss of 0.092W. This results in a maximum core temperature of 52.12C, well within limits.

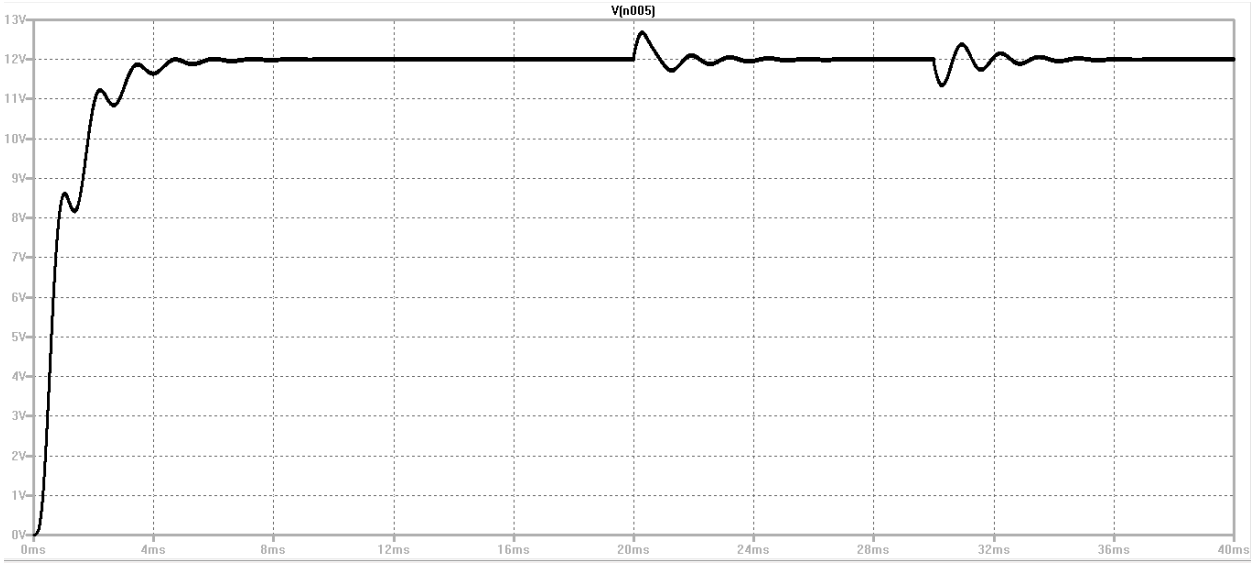
Feedback controller

The feedback controller was derived based on the linearized, averaged model as calculated in Pset 9.1. In simulation, the open-loop buck converter was found to already meet transient output voltage specifications while stepping between minimum and maximum load, for corners of input voltage. Thus, the primary purpose of the feedback controller in this case is to eliminate steady-state error. Because the output voltage ripple is very small, an integral controller is robust and provides stability over the relevant input range. Because the averaged, linearized model has two poles and no zeroes, a relatively high gain can be used to improve settling time without risk of affecting stability.

The feedback controller was implemented as an Integral controller with transfer function

$$\frac{d}{e}(s) = \frac{50}{s}$$

where e(s) is the output voltage error, 12V-V_{out}. This was confirmed via validation to be stable and eliminate steady-state error. In this design, voltage transient never varies more than 6% from the specified voltage output during steps between minimum and maximum load, with a steady-state error of zero. Static voltage specification is met within 600µs. During startup the converter meets this transient specification within 1.8ms. This was verified in LTSPICE using a comparator to generate the PWM signal. The comparator compared a triangle wave source at 100KHz, and a duty cycle signal representing the above transfer function. The duty cycle signal was implemented in SPICE using a behavioral voltage source with voltage output equal to 50 times he integral of 12-V_{out}.



Efficiency Calculation

Efficiency calculation was performed using worst-case power dissipations for both switches and both inductors. Control loss was neglected. Efficiency was calculated to be (150-(.092+3.75+4.237+.7856)/150 = 94%.

Input Voltage Transient Limit

SPICE validation was performed to ensure that for a 44V, 1ms input voltage spike, all components will survive.